

AMENDMENTS TO THE CLAIMS

Claim 1 (Currently Amended): An apparatus for processing data in a spread spectrum system, comprising:

a decimation circuit having an associated decimation factor;

a memory coupled to said decimation circuit; and

an interpolation circuit coupled to said memory, said interpolation circuit having an associated interpolation factor;

wherein said decimation circuit decimates a data rate of received spread spectrum data by said decimation factor to a decimated rate and stores said received data into said memory at said decimated rate; and

wherein said interpolation circuit interpolates said decimated rate by said interpolation factor to an interpolated rate and retrieves said received data from said memory at said interpolated rate.

Claim 2 (Original): The apparatus of claim 1, further comprising:

a communication processor coupled to said interpolation circuit for receiving data from said memory at said interpolated rate.

Claim 3 (Original): The apparatus of claim 1, further comprising:

a dedicated controller for controlling data retrieval from said memory.

Claim 4 (Original): The apparatus of claim 1, further comprising:

a micro-processor for controlling data retrieval from said memory.

Claim 5 (Original): The apparatus of claim 1, wherein said decimation factor is programmable by configuring said decimation circuit.

Claim 6 (Original): The apparatus of claim 1, where in said decimation factor is hard-coded into said decimation circuit.

Claim 13 (Original): The apparatus of claim 12, wherein each of said memory blocks are divided into segments such that data stored in each segment is read out sequentially onto a bussing element accessible by multiple rake fingers via selector circuits in said plurality of despreaders.

Claim 14 (Original): The apparatus of claim 12, wherein said selector circuit includes a block multiplexer, a plurality of sample multiplexers, and a cache coupled to each rake finger.

Claim 15 (Original): The apparatus of claim 1, wherein said memory is a circular buffer.

Claim 16 (Original): The apparatus of claim 15, wherein said circular buffer includes multiple registers.

Claim 17 (Original): The apparatus of claim 16, further comprising a plurality of despreaders.

Claim 18 (Original): The apparatus of claim 17, wherein each of said plurality of despreaders includes:

- a selector circuit; and
- a rake finger.

Claim 19 (Original): The apparatus of claim 18, wherein data stored in said multiple registers are accessible by multiple rake fingers via selector circuits in said plurality of despreaders.

Claim 20 (Currently Amended): An apparatus for processing data in a spread spectrum system, comprising:

- a decimation circuit having an associated decimation factor;
- a memory, which is a circular buffer including multiple registers, coupled to said decimation circuit;
- an interpolation circuit coupled to said memory, said interpolation circuit having an associated interpolation factor; and

a plurality of despreaders, wherein each of said plurality of despreaders includes:
a selector circuit; and
a rake finger;
wherein said decimation circuit decimates a data rate of received data by said decimation factor to a decimated rate and stores said received data into said memory at said decimated rate;
wherein said interpolation circuit interpolates said decimated rate by said interpolation factor to an interpolated rate and retrieves said received data from said memory at said interpolated rate~~The apparatus of claim 18; and~~
_____, wherein said selector circuit includes a first set of multiplexers for selecting in-phase data, a second set of multiplexers for selecting quadrature data, and multiple sample select lines coupled to each rake finger.

Claim 21 (Currently Amended): A method for processing data in a spread spectrum system, comprising the steps of:

receiving spread spectrum data at a sampling rate;
decimating said sampling rate by a decimation factor to obtain a decimated rate;
storing said data into a memory at said decimated rate;
interpolating said decimated rate to obtain an interpolated rate; and
outputting said data from said memory at said interpolated rate to a communication processor.

Claim 22 (Original): The method of claim 21, further comprising the step of:

retrieving data from said memory in accordance with instructions from a micro-processor.

Claim 23 (Original): The method of claim 21, further comprising the step of:

retrieving data from said memory in accordance with instructions from a dedicated controller.

Claim 24 (Original): An apparatus for processing data, comprising:

a plurality of rake fingers;
a memory for storing data at the input to said plurality of rake fingers; and
a selector circuit positioned between said memory and each of said plurality of rake fingers;
wherein said plurality of rake fingers can access said memory substantially simultaneously
via a respective selector circuit, and
wherein said selector circuit includes a first plurality of multiplexers for selecting in-phase
data from said memory, a second plurality of multiplexers for selecting quadrature data from said
memory, and a set of select lines for controlling data being selected by said first plurality of
multiplexers and said second plurality of multiplexers.

Claim 25 (Original): The apparatus of claim 24, wherein said memory is a circular buffer including a plurality of registers.

Claim 26 (Canceled)

Claim 27 (Original): The apparatus of claim 24, wherein said memory is a single-port RAM.

Claim 28 (Currently Amended): An apparatus for processing data, comprising:
a plurality of rake fingers;
a memory, which is a single-port RAM, for storing data at the input to said plurality of rake
fingers; and
a selector circuit positioned between said memory and each of said plurality of rake fingers;
wherein said plurality of rake fingers can access said memory substantially simultaneously
via a respective selector circuit~~The apparatus of claim 27;~~ and
-wherein said memory is divided into memory blocks such that, during each processing
cycle, a first subset of said memory blocks is in a Read mode and a second subset of said memory
blocks is in a Write mode.

Claim 29 (Original): The apparatus of claim 28, wherein each of said memory blocks is divided into segments, such that data stored in each segment is read out sequentially onto a bussing element.

Claim 30 (Original): The apparatus of claim 29, wherein said selector circuit includes a block multiplexer, a plurality of sample multiplexers, and a cache coupled to each rake finger.

Claim 31 (Original): The apparatus of claim 30, wherein said block multiplexer selects a bussing element to receive data from a segment.

Claim 32 (Original): The apparatus of claim 31, wherein said sample multiplexers selects data received from said block multiplexer and stores said data into said cache.

Claim 33 (Original): An apparatus for processing data in spread spectrum systems, comprising:
a memory coupled to a set of despreaders via a bus;
each of said set of despreaders including:
 a block multiplexer coupled to said bus;
 a set of sample multiplexers coupled to said block multiplexer;
 a cache coupled to said sample multiplexers; and
 a rake finger coupled to said cache; and
wherein said set of despreaders can access samples stored in said memory substantially simultaneously via said bus.

Claim 34 (Original): The apparatus of claim 33, wherein said memory is divided into blocks such that during a processing cycle by a desreader, a first subset of said blocks is in a Read mode and a second subset of said blocks is in a Write mode.

Claim 35 (Original): The apparatus of claim 34, wherein said blocks are divided into segments such that samples stored in each of said segments are read out sequentially onto a bussing element coupled to said bus.

Claim 36 (Original): The apparatus of claim 35, wherein said block multiplexer in each of said despreaders selects samples from one bussing element.

Claim 37 (Original): The apparatus of claim 36, wherein said sample multiplexers in each of said despreaders select appropriate Early, On-Time, and Late samples among samples received from said block multiplexer to be stored into said cache.